CLAIMS

What is claimed is:

1 A method for performing a two-step read on a register as an atomic read in a home network, the register having a lower half and an upper half, and is incremented in response to an increment signal and is read in response to a read signal, the method comprising the steps of:

(a) in response to detecting the increment signal, reading the lower half of the register and storing the upper half of the register in a shadow register; and

(b) reading the shadow register to obtain the value of the upper half of the register.

2 The method of claim 1 wherein step (a) further includes the step of: checking for the increment signal when a read request signal is required for the register.

3 The method of claim 2 wherein step (b) further includes the step of: reading the lower half of the register when the read signal is initiated for the register.

4 The method of claim 3 further including the step of providing the register as a count register for maintaining statistics on the home network.

5 The method of claim 4 further including the step of providing the home network with a plurality of count registers.

6 The method of claim 5 further including the step of providing the count registers as 32-bit registers with 16-bit the upper and lower halves.

7 A home network that performs a two-step read on a register as an atomic read, wherein the register has a lower half and an upper half, and is incremented in response to an increment signal and is read in response to a read signal, the home network comprising:

means responsive to detecting the increment signal for reading the lower half of the register and storing the upper half of the register in a shadow register; and

means for reading the shadow register to obtain the value of the upper half of the register.

8 The home network of claim 7 wherein the means responsive to detecting the increment signal further includes means for checking for the increment signal when a read request signal is required for the register.

9 The home network of claim 8 wherein the lower half of the register is read when the read signal is initiated for the register.

10 The home network of claim 9 wherein the register comprises a count register for maintaining statistics on the home network.

11 The home network of claim 10 wherein a plurality of count registers are present.

12 The home network of claim 11 wherein the count registers comprise 32-bit registers with 16-bit the upper and lower halves.

13 A method for performing a two-step read on a count register as an atomic read in a home network, the method comprising the steps of:

(a) providing a plurality of count registers, each having a lower half and an upper half, and each being incremented in response to increment signal and read in response to a read signal;

(b) checking for the increment signal for one of the count registers when a read request signal is required for that count register;

(c) in response to detecting the increment signal, incrementing the count register and deferring sending the read request signal for a cycle;

(d) when the read signal is initiated for the count register, reading the lower half of the count register and storing the upper half of the count register in a shadow register; and

(e) reading the shadow register to obtain the value of the upper half of the count register.

14 The method of claim 13 further including the step of providing the count registers as 32-bit registers with 16-bit the upper and lower halves.

15 A home network comprising;

a control chip for implementing a home phoneline network alliance specification, the control chip including,

a media access controller (MAC), the MAC further including,

at least one shadow register;

a plurality of count registers for maintaining network statistics, each of the count registers including an upper and lower half, and incremented in response to an increment signal; and

a host media access controller program in communication with the MAC for accessing the count registers, wherein the MAC sends a read request signal for the particular count register being read, and wherein before sending the read request signal for the count register,

the MAC checks for the increment signal for the count registers, and in response to detecting the increment signal, the count register is incremented and the MAC defers sending the read request signal for a cycle,

when the MAC sends the read signal for the count register, the lower half of the count register is read and the upper half of the count register is stored in the shadow register, and

the shadow register is to obtain the value of the upper half of the count register.